YGV639

VC1E

Video Controller 1 with Enhanced Functions

■ Outline

YGV639 (hereafter referred to as “VC1E,” its function name) is the display controller which makes it easier to create a highly colorful graphic image in a low-cost system configuration.

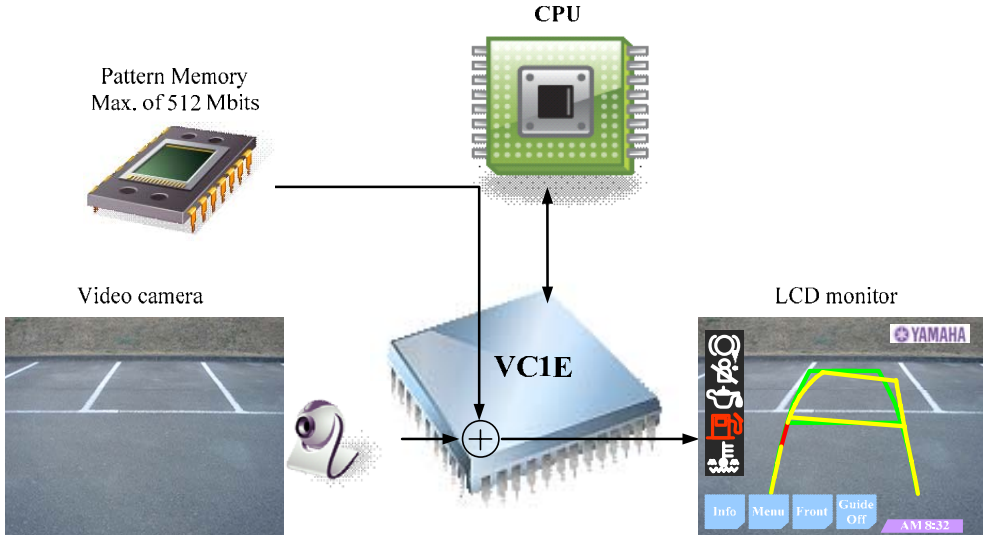
VC1E, having a build-in digital video decode, allows characters, lines, and graphic icons (hereafter, called “sprite”) to be superimposed over CVBS signal from a CCD camera.

It is possible to represent moving images like animation even through a serial port communication, and VC1E realize impressively higher colorful picture expression under an equivalent CPU control load as that of a low-cost OSD controller.

A pattern memory, up to 512M bits (64M bytes), for storing font data or bitmap display data that are used for a sprite, is connectable to VC1E.

A complicated display control program needed to be developed for the conventional graphic controller; however, VC1E allows sprites to be easily displayed only by rewriting the attribute table for display.

VC1E has a build-in line memory for display. For this reason, an external VRAM becomes unnecessary and this allows a system to be built with fewer components.



With recent increase of safety awareness, in-vehicle video cameras are becoming more and more popular. VC1E is best suited for such as parking-support system as would perform superimposition of car-width lines over a video camera footage.

VC1E measures up to the in-vehicle temperature guarantee conditions and can be used also for in-vehicle ECU.

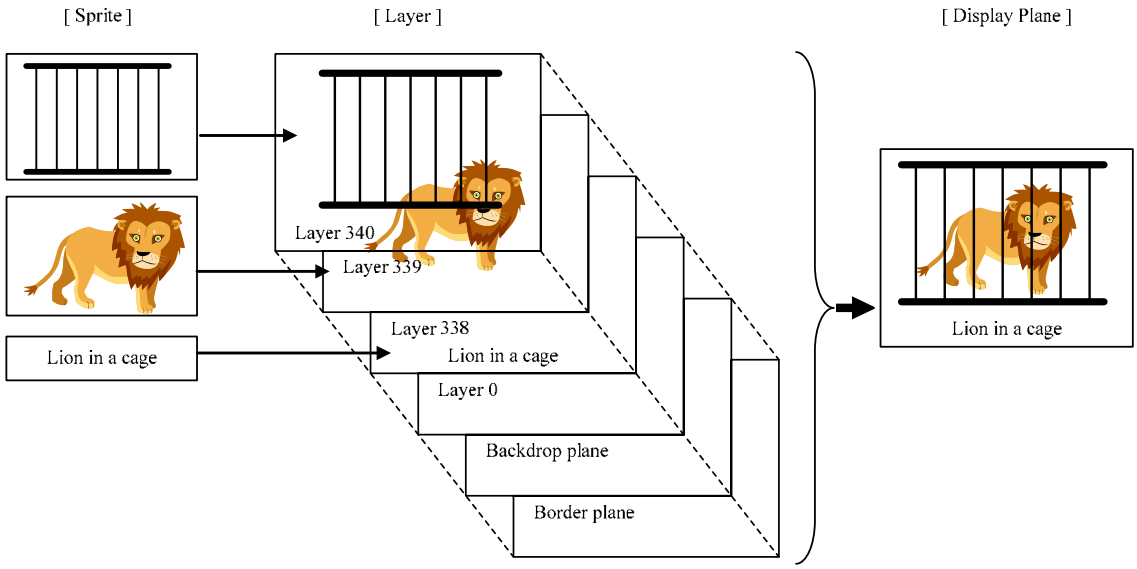
YAMAHA CORPORATION

YGV639 CATALOG
CATALOG No.: LSI-4GV639A30
2010.5

● How VC1E creates an image plane

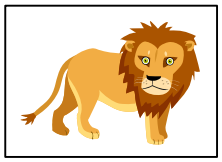
Image Plane Constitution

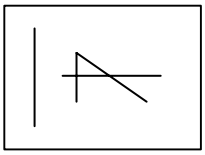
The screen which VC1E displays consists of 341 hierarchical images, called a layer, one backdrop plane, and a border plane with a single color.

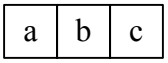


Any one among sprite, two or more lines, and text can be selected in one layer. One sprite, one character string, and lines (up to 510) can be displayed on one layer.

(1) Sprite (2) Two or more lines (3) character string







The display priority order of layers is in order of a layer, a backdrop plane, and a border plane from the top. When a layer or an external video image is not displayed, the border color which is set for the border plane is displayed.

Also when sprites are overlaid and displayed, a lower image comes to appear by setting the surroundings of sprites as a transparent color. Moreover, images can also be overlaid as translucent. This is called alpha blending.

■ Features

Display Function

■ **Monitor supported**
- TFT liquid crystal display (digital RGB connection) or a display equipment with the equivalent I/F

■ **Monitor resolution**
- Programmable for NTSC, PAL, QVGA, WQVGA, VGA, WVGA, SVGA
- Build-in LCD timing controller function

■ **Display plane functions**
- Layered structure up to 341 layers and up to one backdrop plane layer
- Displays sprites, lines and texts by layers
- Alpha-blending control by pixel (alpha by pixel)
- Layer picture quality adjustment function (contrast, brightness)
- Animation by a macro command function

Graphic generation function

■ **Sprite**
- Sprite display: up to 341/field
- Size: 8x8 to 512x512 dots, horizontally and vertically independent selection (in 8-dot unit)
- 2, 16, 32, 64, or 256 palette colors in 64k colors, 65536-color natural picture display by 16-bit RGB natural picture display
- Flip function (vertically and horizontally)
- Scaling function
- Alpha blending in pixels
- Anti aliasing function in the outline part

■ **Text**
- Specifies a font type for each character string
- Supports variable-width fonts such as proportional fonts
- Scaling function
- Supports anti aliasing font

■ **Line drawing**
- Direct drawing by specification of start/end point coordinates (pattern data is not needed)
- Configurable line display up to 510 lines/field
- Display color: 32768-color (RGB555) specification or palette index (10 bits) specification
- Available line width: 1 dot to 16 dots (in dot unit)
- Anti aliasing drawing function

Video Picture Input

■ **Built-in digital video decoder**
- Inputs composite video signals in NTSC/PAL directly and then converts them into digital RGB
- Contrast, brightness, color saturation and hue adjustment function
- Color killer function, video input detection function

■ **Video Picture Input Display Function**
- Scaling function (a function to adjust the resolution of the input image to the display resolution, not a zooming function)
- Mirror inversion function (only horizontal direction)

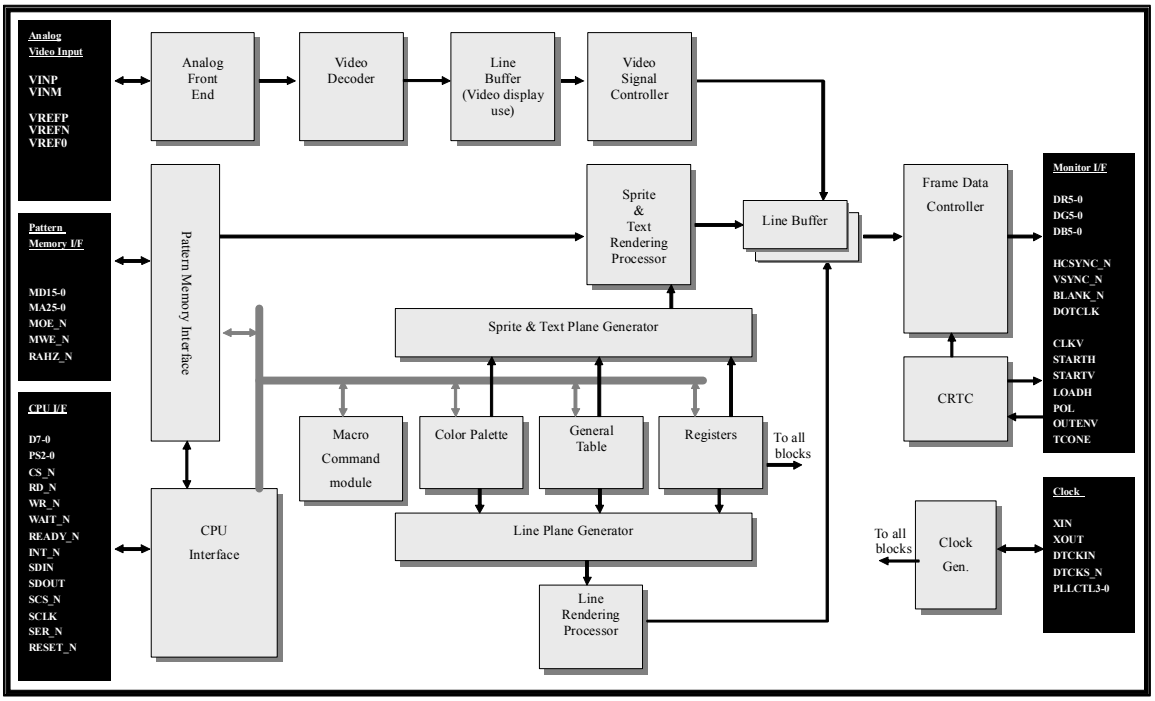
Others

■ **CPU interface**
- 8-bit parallel or serial connection
- Indirect mapping to the built-in registers and tables through the access ports

■ **Pattern memory interface**
- Up to 512M bits (64M bytes), 8-bit/16-bit bus width
- Mask ROM, SRAM, and NOR type flash-memory connectable
- Configurable access timing by the system clock cycle

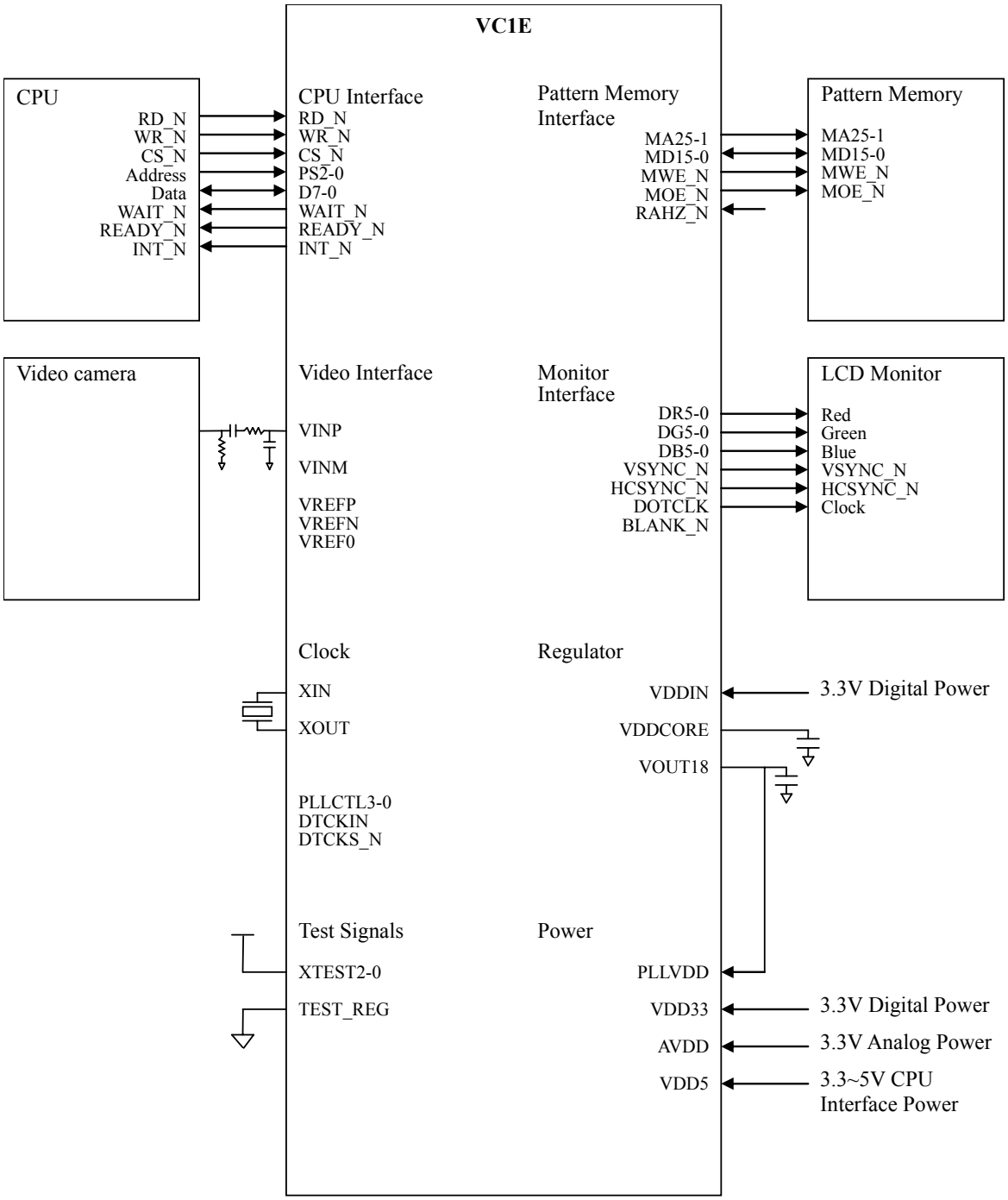
■ **Device specifications**
- 144-pin Lead-free LQFP package (YGV639-VZ)
- CMOS: 3.3V power supply (Built-in regulator for core voltage[1.8V])
- Variable CPU interface power supply (3.3V to 5V)
- Operation temperature range -40℃ to +105℃

■ Block Diagram



Example of System Configuration

An example of a system configuration with VC1E is shown below.



■ Pin Functions

● Pin Table

CPU Interface (23)

Pin Name	Num.	I/O	Function	Attribute	Power Supply Group	Level	Drive
D7-0	8	I/O	CPU data bus	5V tolerant	VD5	CMOS	4mA
PS2-0	3	I	CPU port selection	5V tolerant	VD5	CMOS	
CS_N	1	I	Chip select (dual-purpose pin)	5V tolerant	VD5	CMOS	
RD_N	1	I	Read strobe (dual-purpose pin)	5V tolerant	VD5	CMOS	
WR_N	1	I	Write strobe (dual-purpose pin)	5V tolerant	VD5	CMOS	
WAIT_N	1	OT	CPU bus wait (3-state output) (dual-purpose pin)	5V tolerant	VD5	CMOS	4mA
READY_N	1	OT	CPU bus ready (3-state output)	5V tolerant	VD5	CMOS	4mA
INT_N	1	OD	Interrupt (open drain)	5V tolerant	VD5	CMOS	4mA
SER_N	1	I	CPU interface selection	-	VD3	CMOS	
SCS_N	1	I	Serial interface Chip select (dual-purpose pin)	5V tolerant	VD5	CMOS	
SDIN	1	I	Serial interface Data input (dual-purpose pin)	5V tolerant	VD5	CMOS	
SDOUT	1	OT	Serial interface Data output (3-state output) (dual-purpose pin)	5V tolerant	VD5	CMOS	4mA
SCLK	1	I	Serial clock input (dual-purpose pin)	5V tolerant	VD5	CMOS	
RESET_N	1	I$	Reset	Tolerant	VD3	CMOS	

Pattern Memory Interface (45)

Pin Name	Num.	I/O	Function	Power Supply Group	Level	Drive
MD15-0	16	I/O	Pattern memory Data Bus	VD3	LVCMOS	4mA
MA25-0	26	OT	Pattern memory Address Bus (3-state output)	VD3	LVCMOS	4mA
MOE_N	1	OT	Pattern memory Output Enable (3-state output)	VD3	LVCMOS	4mA
MWE_N	1	OT	Pattern memory Write Strobe (3-state output)	VD3	LVCMOS	4mA
RAHZ_N	1	I	Pattern memory high-impedance switching	VD3	LVCMOS	

Video Interface (5)

Pin Name	Num.	I/O	Function	Attribute	Power Supply Group	Level	Drive
VINP	1	I	Analog video input	Analog	AVDD	Analog	
VINM	1	I	Test input pin	Analog	AVDD	Analog	
VREF0	1	O	ADC reference pin	Analog	AVDD	Analog	
VREFP	1	O	Plus reference voltage pin for ADC	Analog	AVDD	Analog	
VREFN	1	O	Minus reference voltage pin for ADC	Analog	AVDD	Analog	

Monitor Interface (29)

Pin Name	Num.	I/O	Function	Power Supply Group	Level	Drive
DR5-0	6	O	Digital Video: R Output	VD3	LVCMOS	2mA
DG5-0	6	O	Digital Video: G Output	VD3	LVCMOS	2mA
DB5-0	6	O	Digital Video: B Output	VD3	LVCMOS	2mA
VSYNC_N	1	O	Vertical synchronization signal output (dual-purpose pin)	VD3	LVCMOS	2mA
HCSYNC_N	1	O	Horizontal / Composite synchronization signal output (dual-purpose pin)	VD3	LVCMOS	2mA
BLANK_N	1	O	Blank signal output pin (dual-purpose pin)	VD3	LVCMOS	2mA
DOTCLK	1	O	Dot clock output	VD3	LVCMOS	2mA
CLKV	1	O	Vertical clock output (dual-purpose pin)	VD3	LVCMOS	2mA
STARTH	1	I/O	Horizontal start signal output (dual-purpose pin)	VD3	LVCMOS	2mA
STARTV	1	O	Vertical start signal output (dual-purpose pin)	VD3	LVCMOS	2mA
LOADH	1	O	Horizontal load signal output (dual-purpose pin)	VD3	LVCMOS	2mA
POL	1	O	Polarity inversion output (dual-purpose pin)	VD3	LVCMOS	2mA
OUTENV	1	O	Output enable signal (dual-purpose pin)	VD3	LVCMOS	2mA
TCONE	1	I	Timing controller select pin (with a pull-down resistor)	VD3	LVCMOS	

Clock (8)

Pin Name	Num.	I/O	Function	Power Supply Group	Level	Drive
XIN	1	I	Reference clock input pin	VD3		
XOUT	1	O	Crystal connection pin	VD3		
DTCKIN	1	I	Dot clock input pin	VD3	LVCMOS	
DTCKS_N	1	I	Dot clock input selection pin	VD3	LVCMOS	
PLLCTL3-1	3	I/O	PLL multiplication ratio setting pin (dual-purpose pin)	VD3	LVCMOS	2mA
PLLCTL0	1	I	PLL multiplication ratio setting pin	VD3	LVCMOS	

For Device (43)

Pin Name	Num.	I/O	Function	Attribute	Power Supply Group	Level	Drive
XTEST2-0	3	I	Test pin	-	VD3	LVCMOS	
VDD33	11	-	Digital power supply pin	-	-		
VDD5	1	-	CPU interface power supply pin	-	-		
VSS	14	-	Digital VSS pin	-	-		
PLLVDD	1	-	PLL power supply pin	-	-		
AVDD1, AVDD2	2	-	Analog Front End power supply pin	-	-		
AVSS	2	-	Analog Front End VSS pin	-	-		
OCPEN	1	I	Reset of the over-current protection circuit Over-current protection circuit Enable/Disable switching pin	5V tolerant	VD5	CMOS	
TEST_REG	1	I	Over-current protection circuit Enable/Disable control	5V tolerant	VD5	CMOS	
OCP_N	1	O	Over-current detection output	-	VD5	CMOS	4mA
VDDCORE	3	-	Capacitor connection pin for core power supply	-	VDDIN		
VOUT18	1	-	1.8V digital power supply output	-	VDDIN		
VDDIN	2	-	3.3V input for core power supply (1.8V)	-	-		

Note: VC1E has no pull-up resistors. Pull up a pin externally as necessary.

- The meaning of a sign of [I/O] column is as follows:
  I: Input pin I$: Schmitt trigger input pin
  O: Output pin OT: 3-state output pin OD: Open-drain output pin

- The meaning of [Attribute] column is as follows:
  - Analog: analog pin
  - tolerant: tolerant attribute represents that current does not flow to a power supply pin from the voltage-applied pin, when voltage higher than supply voltage is applied to the pin.
    However, since this pin cannot withstand 5V, it is necessary to make the voltage difference between the pin and the power supply voltage less than 3.6V. Therefore, voltage exceeding 3.6V (maximum of recommended operation voltage) cannot be applied to it without the supply of power (supply voltage = 0V).
  - 5V tolerant: 5V tolerant attribute means the pin has a withstand voltage of 5V. That is, 5V can be applied to this pin when supply voltage is 0V.

Dual-purpose Pin

Sharing CPU Interface Pins

VC1E supports the two types of CPU interfaces: serial and parallel interfaces. Pins are shared by the interfaces as follows:

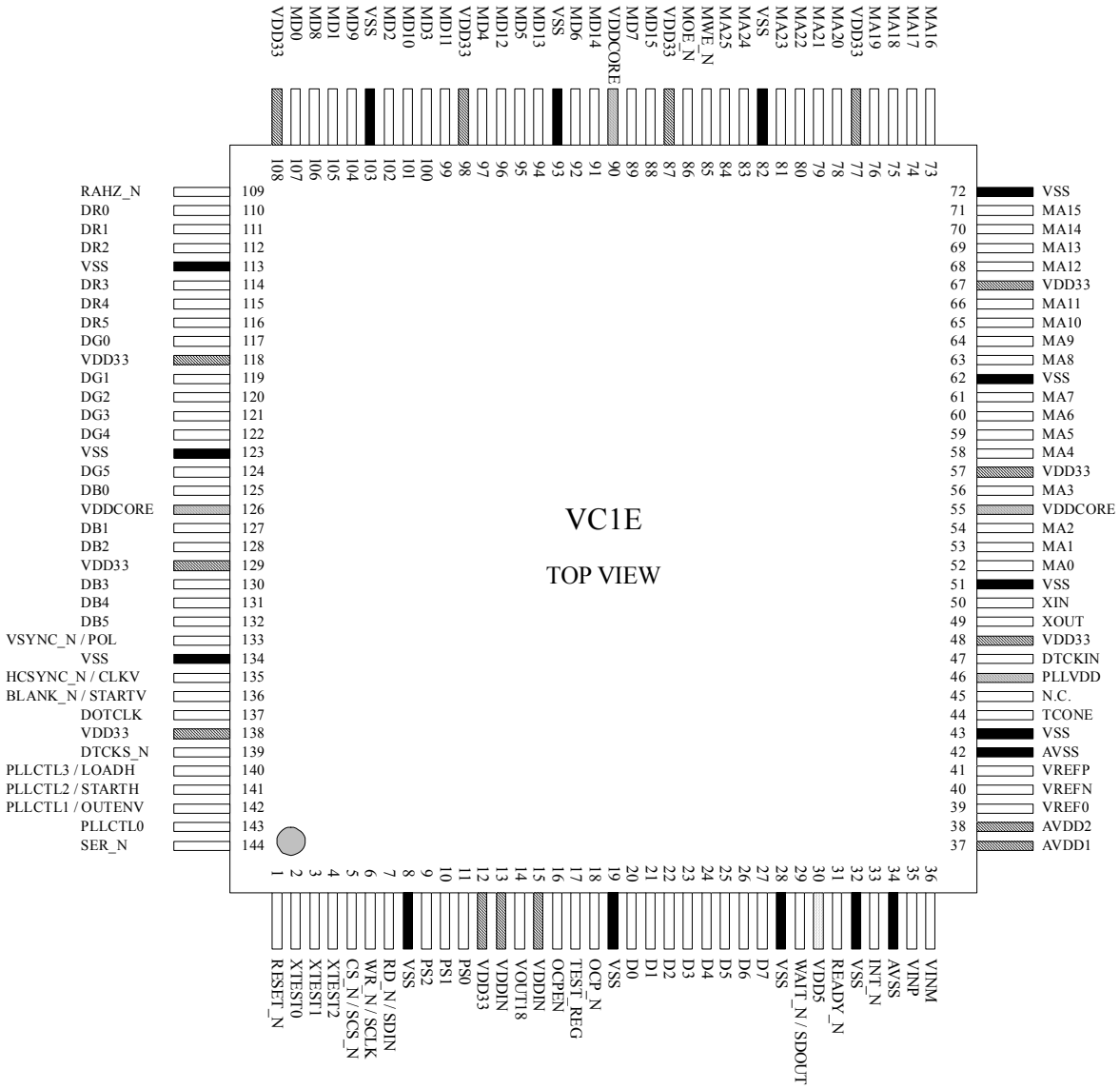
Pin Name	Parallel Interface (SER_N=H)	Serial Interface Chip Select (SER_N=L)
D7-0	D7-0	Unused
PS2-0	PS2-0	Unused
CS_N	CS_N	SCS_N
RD_N	RD_N	SDIN
WR_N	WR_N	SCLK
WAIT_N	WAIT_N	SDOUT
READY_N	READY_N	Unused
INT_N	INT_N	INT_N

Sharing Timing-Controller Pins

VC1E has a built-in LCD timing controller and this function can be enabled by TCONE pin setting. The following pins are shared depending on whether the timing controller is enabled or disabled.

Pin Name	Timing controller disabled (TCONE=L)	Timing controller enabled (TCONE=H)
DR5-0	DR5-0	DR5-0
DG5-0	DG5-0	DG5-0
DB5-0	DB5-0	DB5-0
DOTCLK	DOTCLK	DOTCLK
HCSYNC_N	HCSYNC_N	CLKV
VSYNC_N	VSYNC_N	POL
BLANK_N	BLANK_N	STARTV
PLLCTL3	PLLCTL3	LOADH
PLLCTL2	PLLCTL2	STARTH
PLLCTL1	PLLCTL1	OUTENV

● Pin Arrangement



Note: N.C. (pin 45) is a no connection pin, with only lead frame, and no bonding wire is connected.

■ Description of Pin Function

Power Supply

Digital Power Supply Pins

VDD33, VDDIN, VSS (Power Supply)

The power supply pins for the internal digital circuit. Supply 3.3V to VDD33 and VDDIN pins. Supply the ground level to VSS pins.

It is recommended to decouple VDD33 and VDDIN with respect to the ground through a high-frequency ceramic capacitor. The decoupling capacitor should be positioned between VDD33 and VSS, VDDIN and VSS as close to the device as possible so that the wiring length becomes the shortest.

Power Supply Pin for PLL

PLLVDD (Power Supply)

This is the analog power supply pin for VCO of the built-in PLL. Connect VOUT18 pin to PLLVDD pin. Connect a decoupling capacitor between this PLLVDD and the VSS (Pin 43).

Power Supply Pins for Analog Front End

AVDD1, AVDD2, AVSS (Power Supply)

This is the analog power supply pin for the built-in Analog Front End. Supply 3.3V to AVDD1 and AVDD2 pins. Supply the ground level to AVSS pins. These power supplies should be separated from the other power supplies. It is recommended that this pin should be decoupled by a high-frequency ceramic capacitor to the analog ground. A decoupling capacitor should be positioned between AVDD1 (pin 37) and AVSS (pin 34), AVDD2 (pin 38) and AVSS (pin 42) as close to the device as possible so that the wiring length becomes shortest.

Inside the LSI, AVDD1 is connected to an AD converter and AVDD2 is connected to a clamping circuit or a reference voltage circuit. AVDD1 generates about 27 MHz switching noise. Therefore, it is recommended to take measures, such as insertion of different ferrite beads to AVDD1 and AVDD2, so that noise may not input to AVDD2 through AVDD1.

Power Supply Pin for CPU Interface

VDD5 (Power Supply)

This is the power supply pin for the level shifter of CPU interface. It is possible to input 3.3V to 5V according to CPU interface voltage. Connect a decoupling capacitor between this pin (VDD5) and VSS pin.

System Reset

Reset Pin

RESET_N (Schmitt Trigger Input)

This is the power-on reset input pin. The reset signal must be input for a given time after power on. This pin is low active. The pin uses a schmitt trigger type buffer

Clock

There are three clocks which are used in VC1E.

(1) Dot Clock : clock for picture display and picture data output.
(2) System Clock : internal clock (about 81MHz) for picture processing in VC1E.
(3) Decoder Clock : internal clock (about 27MHz) that is used when decoding analog video signals.

These three clocks can be generated from a single crystal resonator.

PLL Reference Clock Crystal Connection Pins

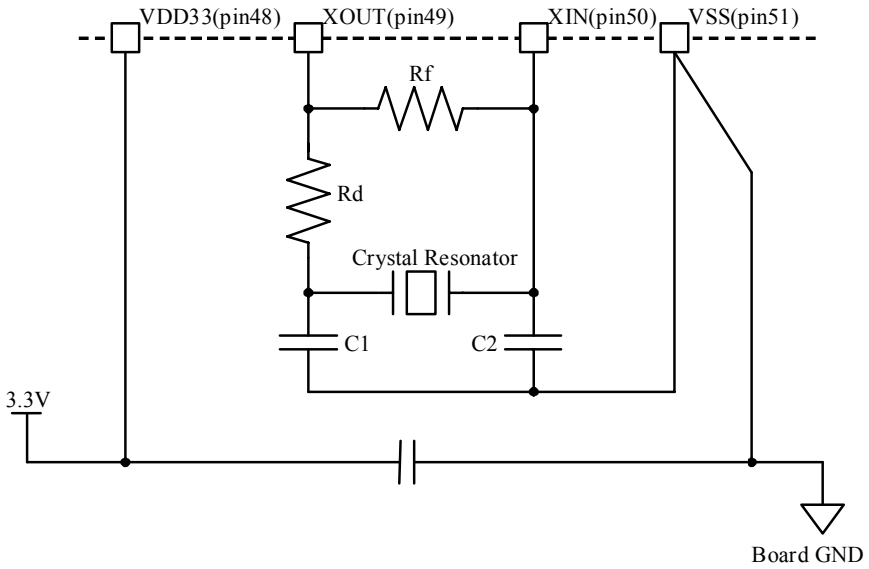
XIN (Input), XOUT (Output)

VC1E oscillates clocks by connecting a crystal resonator to XIN and XOUT pins. When using the externally-oscillated clock, input it to XIN pin. In this case, nothing should be connection to XOUT pin.

When generating a dot clock, system clock and decoder clock from a single clock input, connect a crystal resonator of the same frequency as that of the dot clock to this XIN pin or input the clock.

- The frequency that can be oscillated with XIN and XOUT pins is 6MHz to 30MHz.
- The clock frequency that can be input to XIN pin ranges from 6MHz to 40MHz.

Below is shown the external circuit for the clock oscillation with a crystal resonator.



- C1, C2: External load capacity
- Rf: Feedback resistor
- Rd: Damping resistor

■ Reference values of the oscillator circuit constants

Crystal Resonator	KYOCERA KINSEKI CX8045GB 8MHz	KYOCERA KINSEKI CX8045GB 14MHz
Rf	1M Ω	1M Ω
Rd	1.6k Ω	820 Ω
C1, C2	12pF	12pF

Note: The above constants do not always guarantee the oscillation as they are the reference values based on the evaluation under the particular circumstance. For actual application, please ask the resonator's manufacturer to evaluate the resonator with it mounted on a board.

In order to secure stable operation of the oscillation circuit, it is recommended to take the following measures for preventing noise.

(1) LSI and crystal resonator, etc. should be placed as close to each other as possible to shorten the length of wiring.
(2) GND of the oscillation circuit must be directly connected to VSS(pin51) of the LSI.
(3) The oscillation circuit must be separated from a wiring pattern in which a large current flows.

(4) Connect a decoupling capacitor between VDD33(pin48) and VSS(pin51).
(5) Board's GND pattern must be wide enough to prevent the interference from other signals. Connect this GND to VSS(pin51).

VC1E's electrical characteristics were determined based on the assumption that a X'tal resonator is to be connected to XIN/XOUT or X'tal oscillator is to XIN. Therefore, it is recommended to use a crystal resonator or crystal oscillator. Use a X'tal resonator or X'tal oscillator with the allowable frequency deviation (including temperature characteristics) of ±100ppm.

■ Ceramic Resonator

If using a ceramic resonator, the following points should be considered.

- Use a ceramic resonator with the same jitter performance as that of a crystal resonator.
- Ceramic resonators have relatively bigger allowable frequency deviation and frequency temperature characteristics than those of a crystal resonator.

Such variation is not considered in the design; therefore, the system clock frequency should be within the range of the specification (83.16MHz or less for VC1E) even if the frequency varies.

Dot Clock Input Pin

DTCKIN (Input)

When a dot clock is present in the system, this dot clock can be directly input to DTCKIN pin as a dot clock.

The pin input is enabled when DTCKS_N="L." When DTCKS_N="H," a dot clock is generated by the clock input to XIN pin. At this time, connect VDD33 or GND to DTCKIN pin. A clock frequency up to 40MHz can be input into DTCKIN pin.

Dot Clock Input Select Pin

DTCKS_N (Input)

This is the pin to select which one of either XIN or DTCKIN pin should be used for supplying the internal dot clock. This pin is low active. Be sure to determine the level of the input signal to this pin during the reset (RESET_N pin="L") at power-on, and do not change the state while the power has been already established.

PLL Control Pin

PLLCTL3-0 (Input)

These pins set a multiplication ratio of the built-in PLL that generates a system clock. Be sure to determine the level of the input signals to the pins during the reset (RESET_N pin="L") at power-on, and do not change the state while the power has been already established. PLLCTL3-1 are dual-purpose pins for LOADH, STARTH, and OUTENV, respectively. When using a built-in timing controller, it functions as LOADH, SHARTH, and OUTENV.

CPU Interface

Although in VC1E either 8-bit asynchronous parallel or synchronous serial interface can be selected, pins are shared by both interfaces.

CPU Data Bus

D7-0 (Input and Output)

When using 8-bit parallel interface, connect these pins to the CPU data bus. D7-0 serve as output pins when both CS_N and RD_N pins are asserted ("L" level input), otherwise, it serves as input pins. Pull up D7-0 pins outside the device as no pull-up resistors are provided.

When using the serial interface, input "H" or "L" level to the pins.

Port Select Pins

PS2-0 (Input)

Internal port selection pins. Connect the pins to the CPU address bus when 8-bit parallel interface is used.

When using VC1E in serial interface, input "H" or "L" level to the pins.

Chip Select Pin

CS_N (Input)

Chip-select input pin when 8-bit parallel interface is selected. WR_N and RD_N pins are enabled when this signal is in active state. Connect CS_N pin to the CPU's chip select pin for external devices. This pin is low active. This pin is a dual-purpose pin. When using the serial interface, it functions as SCS_N pin.

Read Strobe Input Pin

RD_N (Input)

Read Strobe Input Pin when 8-bit parallel interface is used. This pin is Low-active. This pin is a dual-purpose pin. When using the serial interface, it functions as SDIN pin.

Write Strobe Input Pin

WR_N (Input)

Write Strobe Input Pin when 8-bit parallel interface is used. This pin is low active. This pin is a dual-purpose pin. When using the serial interface, it functions as SCLK pin.

CPU Bus Wait Pin

WAIT_N (3-State Output)

The bus wait signal is output when 8-bit parallel interface is used. Use this pin and READY_N pin properly depending on CPU. This pin is a 3-state output.

While "H" level is input to CS_N pin, it becomes a high impedance state. This pin is low active. Pull up this pin outside the device as no pull-up resistor is provided. This pin is a dual-purpose pin. When using the serial interface, it functions as SDOUT pin.

CPU Bus Ready Pin

READY_N (3-State Output)

The bus ready signal is output when 8-bit parallel interface is used. Use this pin and WAIT_N pin properly depending on CPU. This pin is a 3-state output. While "H" level is input to CS_N pin, it becomes a high impedance state. This pin is low active. Pull up READY_N pin outside the device as no pull-up resistor is provided.

Interrupt Pin

INT_N (Open Drain Output)

An interrupt request signal is output. INT_N signal is asserted when a flag enabled by the internal register is set to "1." When the flag is reset by the writing to the flag bit or when the interrupt enable bit is set to "0," INT_N signal is negated and becomes high impedance state. This pin is low active. Since this pin is an open-drain output, a wired-OR connection with similar interrupt signals can be made. Pull up INT_N pin outside the device as no pull-up resistor is provided.

CPU Interface Select Pin

SER_N (Input)

CPU interface selection pin. When choosing the serial interface, set to "L." When choosing the parallel interface, set to "H." This pin is low active.

An input signal level should be settled during the period of RESET_N pin="L" at power-on and must not be changed while the power is ON.

Serial Interface Chip Select Input Pin

SCS_N (Input)

This is used as the chip select input pin when serial interface is selected. SDIN and SCLK pins become enabled when this signal is in active state. This pin is low active.

This pin is a dual-purpose pin. When using the parallel Interface, it functions as CS_N pin.

Serial Data Input Pin

SDIN (Input)

This pin is used as the serial data input pin when serial interface is selected.

This pin is a dual-purpose pin. When using the parallel Interface, it functions as RD_N pin.

Serial Data Output Pin

SDOUT (3-State Output)

This pin is used as the serial data output pin when serial interface is selected.

This pin is a dual-purpose pin. When using the parallel interface, it functions as WAIT_N pin.

Serial Clock Input Pin

SCLK (Input)

This pin is used as the serial clock input pin when serial interface is selected.

This pin is a dual-purpose pin. When using the parallel interface, it functions as WR_N pin.

Pattern Memory Interface

These pins are used for interface with a pattern memory connected to VC1E local buses. Mask-ROM, NOR-type flash memory and SRAM, etc. can be connected as a pattern memory.

Pattern Memory Data Bus

MD15-0 (Input and Output)

Data input-output bus for a pattern memory. When the data bus width of a pattern memory is 16 bits, connect an external memory to MD15-0. When the data bus width is 8 bits, connect an external memory to MD7-0 and pull up MD15-8. The data bus width of a pattern memory is set by the register (R#5: BW).

MD15-0 serve as output pins only for the write access to a pattern memory; otherwise, they serve as input pins. However, when the pattern memory bus is set to 8 bits, MD15-8 serve as input pins, even in the write access.

MD15-0 pins become high impedance when RAHZ_N= "L." And, when core power supply is shut down with the activation of the over current protection circuit, this pin becomes high impedance due to the voltage decrease.

It is recommended to connect an external pull-up resistor of 10kΩ to 50kΩ to this pin.

Pattern Memory Address Bus

MA25-0 (3-State Output)

Address bus output pins for the pattern memory. When the data bus width of a pattern memory is 16 bits, connect it to MA25-1. When the width is 8 bits, connect it to MA25-0. When RAHZ_N is "L" level or when core power supply is shut down by the overcurrent protection circuit in the internal regulator, MA25-0 pins become high impedance.

Pattern Memory Output Enable Pin

MOE_N (3-State Output)

Pattern memory output enable pin. This pin is low active.

When RAHZ_N is "L" level, MOE_N pin becomes high impedance. And, when core power supply is shut down with the activation of the over current protection circuit, this pin becomes high impedance due to the voltage decrease. It is recommended to attach an external pull-up resistor 10kΩ to 50kΩ to this pin.

Pattern Memory Write Strobe Output Pin

MWE_N (3-State Output)

Writing enable output pin for pattern memory. This pin is low active.

When RAHZ_N is "L" level, MWE_N pin becomes high impedance. And, when core power supply is shut down with the activation of the over current protection circuit, this pin becomes high impedance due to the voltage decrease. It is recommended to attach an external pull-up resistor 10kΩ to 50kΩ to this pin.

Pattern Memory High-Impedance Switching Pin

RAHZ_N (Input)

Sets the Interface pins for the pattern memory to high impedance. Assert this pin to separate the pattern memory electrically from VC1E. This pin is low active.

Monitor Interface

These pins output picture data or timing signals to an external monitor.

Digital Picture Interface Pins

DR5-0, DG5-0, DB5-0 (Output)

These pins output digital R, G, and B signals of display data in synchronization with DOTCLK.

Vertical Synchronization Signal Output Pin

VSYNC_N (Output)

The vertical sync signal is output in synchronization with DOTCLK.

This pin's activation state is selectable by the register setting.

- When the register (R#6:REVSY) is "0": Low-active
- When the register (R#6:REVSY) is "1": High-active

This pin is dual-purpose pin. When using the built-in timing controller, it functions as POL.

Horizontal / Composite Synchronization Signal Output Pin

HCSYNC_N (Output)

Horizontal or composite sync signal is output in synchronization with DOTCLK. Which signal should be output is specified by the resistor (R#6: CSYOE).

This pin's activation state is selectable by the register setting.

- When the register (R#6:REVSY) is "0": Low-active
- When the register (R#6:REVSY) is "1": High-active

This pin is dual-purpose pin. When using the built-in timing controller, it functions as CLKV.

Blank Signal Output Pin

BLANK_N (Output)

A signal that indicates a blank period is output in synchronization with DOTCLK. This signal can be used when needing the signal (DE) which indicates a display period in an LCD panel etc.

This pin is dual-purpose pin. When using the built-in timing controller, it functions as STARTV.

Dot Clock Output Pin

DOTCLK (Output)

This pin outputs a dot clock. The dot clock used in VC1E is output. The following three ways are selectable.

(1) Outputs an input clock to XIN pin as is or in frequency-divided form
(2) Outputs a PLL output clock as is or in frequency-divided form
(3) Outputs an input clock to DTCKIN pin as is

DOTCLK has the inversion output function. This is implemented by selecting the clock reversed by the group selector just before outputting an internal dot clock to DOTCLK pin. Set DOTCLK inversion function so that it meets each signal's Set-up/Hold time regulation of your monitor with respect to DOTCLK.

This pin output optimizes the drive capability to QVGA, dotclock frequency of approx. 6.36MHz. When using a dot clock frequency of approx. 20MHz or more, it is recommended to add a clock buffer to the board. And, when LCD's input capacitance is large, the waveform may get distorted; therefore, check the waveform by using an actual terminal.

Vertical Clock Output Pin

CLKV (Output)

When using the built-in timing controller, it outputs a vertical clock. This pin is dual-purpose pin. When not using the built-in timing controller, it functions as HCSYNC_N.

Horizontal Start Signal Output Pin

STARTH (Output)

When using the built-in timing controller, it outputs a horizontal start signal.
This pin's activation state is selectable by the register setting.

- When the register (R#111: REVSH) is "0": High-active
- When the register (R#111: REVSH) is "1": Low-active

This pin is dual-purpose pin. When not using the built-in timing controller, it functions as PLLCTL2.

Vertical Start Signal Output Pin

STARTV (Output)

When using the built-in timing controller, it outputs a vertical start signal.
This signal's activation state is selectable by the register setting.

- When the register (R#112: REVSV) is "0": High-active
- When the register (R#112: REVSV) is "1": Low-active

This pin is dual-purpose pin. When not using the built-in timing controller, it functions as BLANK_N.

Horizontal Load Signal Output Pin

LOADH (Output)

When using the built-in timing controller, it outputs a horizontal load signal.
This signal's activation state is selectable by the register setting.

- When the register (R#111: REVLH) is "0": High-active
- When the register (R#111: REVLH) is "1": Low-active

This pin is dual-purpose pin. When not using the built-in timing controller, it functions as PLLCTL3.

Polarity Invert Signal Output Pin

STARTH (Output)

When using the built-in timing controller, it outputs a polarity invert signal. This pin is dual-purpose pin.
When not using the built-in timing controller, it functions as VSYNC_N.

Output Enable Signal

OUTENV (Output)

When using the built-in timing controller, it outputs an output-enable signal. This pin is dual-purpose pin.
When not using the built-in timing controller, it functions as PLLCTL1.

Timing Controller Select Pin

TCONE (Input)

This is a select pin for the built-in timing controller. If this TCONE pin is connected to "VDD33", the timing signal to be output from a built-in timing controller will be output to a dual-purpose pin.

An input signal level should be settled during the period of RESET_N pin="L" at power-on and must not be changed while the power is ON. Although a pull-down resistor is included, it is recommended to connect this pin to GND when using it with TCONE=L. When using with TCONE=H, this pin should be connected to VDD33 without the resistor.

Power Regulator Pins for Core

VC1E has the built in regulator for core power supply. And over current protection circuit to detect a short circuit is also incorporated.

Over Current Protection Circuit Reset Pin

OCPEN (Input)

Enables/Disables the operation of the over current protection circuit.

- "H" input: Enable operation of over current protection circuit.
- "L" input: Disable operation of over current protection circuit.

This signal shuts down the power supply regulator output temporarily when detecting an over-current condition.

OCPEN functions as the reset signal of the over current protection circuit. When "L" is input to OCPEN, power is supplied again.

Over Current Protection Circuit Enable Pin

TEST_REG (Input)

This is the test pin for the over current protection circuit. Normally, this pin should be used with it held to "L."

Output of Over Current Detection State

OCP_N (Output)

This signal indicates the state of the over current protection circuit. Connect this pin to a CPU port etc. to monitor its state.

- "L" output: The regulator shuts down the core power supply by detecting an over current condition.
- "H" output: The regulator outputs the power as normal operation.

OCP_N pin becomes "L" level when the voltage of the core power supply output pin VOUT18 is low, such as at power-on or power supply recovery from the shutdown state due to overcurrent detection, etc.

Capacitor Connection Pin for Core Power Supply

VDDCORE

The decoupling capacitor connection pins for core power supply. Connect a 4.7µF ceramic capacitor between VDDCORE and GND. Put the capacitor as close to VDDCORE pin as possible.

Note: Do not supply power to this VDDCORE pin.

1.8V Power Output Pin

VOUT18 (Output)

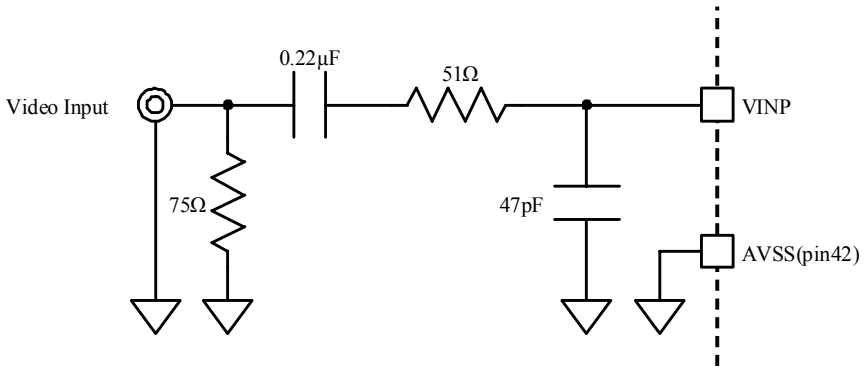
1.8V-power-supply regulator output pin. Connect it to PLLVDD pin. Connect a 4.7µF ceramic capacitor between VOUT18 and GND. Put the capacitor as close to VOUT18 pin as possible.

Analog Front End

Analog Video Input

VINP (Input)

Analog video input pin. Input composite video signals to this pin.

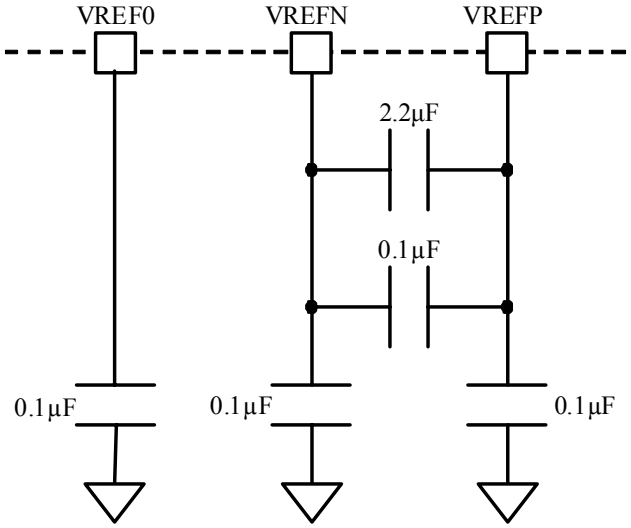


Use laminated ceramic capacitors (capacitance tolerance: ±10%, temperature coefficient: ±15%) or those having higher characteristics.

Reference Voltage Pins for ADC

VREFP, VREFN, VREF0 (Output)

These pins are for generating a reference voltage inside Analog Front End. Connect a capacitor externally.



Use laminated ceramic capacitors (capacitance tolerance: ±10%, temperature coefficient: ±15%) or those of higher characteristics except for the 2.2µF capacitor.

Test Differential Input Pin

VINM (Input)

This is a test pin. This signal functions as a differential input pin of VINP input at the test. Normally connect it to AVSS.

Other Control Pins

For Device Test Pin

XTEST2-0 (Input)

These are the test mode setting pins for device test. Be sure to use them in the following setting.

Pin Name	XTEST2	XTEST1	XTEST0
Input level	H	H	H

Note that if the device is used outside the specified level, the device itself or the system using it may be damaged significantly.

■ Electrical Characteristics

● Absolute Maximum Ratings

Items	Symbol	Rating	Unit	Note
Supply voltage (VDD5 pin)	V_{DD5}	-0.5 to +7.0	V	1
Supply voltage (VDD33, VDDIN pin)	V_{DD33}	-0.5 to +4.6	V	1
Analog Supply Voltage (AVDD pin)	V_{AVD}	-0.5 to +4.6	V	1
PLL Supply Voltage (PLLVDD pin)	V_{PLVD}	-0.5 to +2.5	V	1
Input Pin Voltage (VDD5 power supply pin)	V_I	-0.5 to +7.0	V	1
Input Pin Voltage (RESET_N pin)	V_I	-0.5 to VDD33+4.6 (≤5.5 Max.)	V	1
Input Pin Voltage (VDD33 power supply pin other than RESET_N)	V_I	-0.5 to VDD33+0.5 (≤4.6 Max.)	V	1
Input Pin Voltage (AVDD power supply pin)	V_I	-0.5 to AVDD+0.5 (≤4.6 Max.)	V	1
Output Pin Voltage (including VDD5 power supply, tolerant pin, and input/output pins)	V_O	-0.5 to +5.5	V	1
Output Pin Voltage (Other VDD5 power supply pin)	V_O	-0.5 to VDD5+0.5 (≤5.5 Max.)	V	1
Output Pin Voltage (including VDD33 power supply pin and input/output pins)	V_O	-0.5 to VDD33+0.5 (≤4.6 Max.)	V	1
Output Pin Voltage (including AVDD power supply pin and input/output pins)	V_O	-0.5 to AVDD+0.5 (≤4.6 Max.)	V	1
Input Pin Current	I_I	-20 to +20	mA	
Output Pin Current	I_O	-20 to +20	mA	
Storage Temperature	T_{STG}	-50 to +125	℃	

Note) Refer to “Pin Table” for the details of the power supply pin and the attribute.
Note 1) Values are based on VSS(GND)=0V

● Recommended Operating Condition

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Power-supply Voltage (VDD33, VDDIN pins)	V_{DD33}	3.0	3.3	3.6	V	1
Analog Power Supply (AVDD pins)	V_{AVD}	3.0	3.3	3.6	V	1
PLL Power Supply (PLLVDD pins)	V_{PLVD}	1.65	1.8	1.95	V	1, 2
CPU I/F Power Supply (VDD5 pins)	V_{DD5}	3.0	5.0	5.25	V	1
Operating Ambient Temperature	T_{OP}	-40		105	℃	3

Note 1) Values are based on VSS(GND)=0V.
Note 2) PLLVDD pin should be connected to VOUT18 pin. No need to prepare an external 1.8V power supply.
Note 3) This value is estimated with the following conditions:
・Four-layer substrate with the size of more than 100 mm × 120 mm
・Copper-thin film area ratio over 300%
・No solder applied between Stage and Substrate

● Consumption Current

Items	Conditions	Symbol	Min.	Typ	Max.	Unit	Note
Total Power Consumption	C_L=20pF V_{IL}=GND V_{IH}=V_{DD33}	P_D			544	mW	1
Consumption Current Breakdown							
VDD33, VDDIN		I_{VDD}			120	mA	1, 2
VDD5		I_{VDD5}			7.5	mA	1
AVDD		I_{AVD}			20	mA	1

Note 1) Consumption current and consumption power values are the values measured under the recommended operating condition.
Note 2) The current flowing through PLLVDD pin is included in VDD33’s and VDDIN’s current values because it is generated by the internal regulator.

● DC Characteristics

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Low Level Input Voltage						
XIN pin	V_{IL}	-0.3		V_{DD33}×0.3	V	1
Power Supply Group "VD3" input and I/O pins (Except XIN pin)	V_{IL}	-0.3		0.8	V	1,2
Power Supply Group "VD5" input and I/O pins at VDD5=3.0 to 3.6V	V_{IL}	-0.3		V_{DD5}×0.2	V	1,3
Power Supply Group "VD5" input and I/O pins at VDD5=3.6 to 5.25V	V_{IL}	-0.3		0.8	V	1,3
High Level Input Voltage						
XIN pin	V_{IH}	V_{DD33}×0.7		V_{DD33}+0.3	V	1
Power Supply Group "VD3" input and I/O pins (Except XIN pin)	V_{IH}	2.0		3.6	V	1,2
Power Supply Group "VD5" input and I/O pins at VDD5=3.0 to 3.6V	V_{IH}	V_{DD5}×0.8		V_{DD5}+0.3	V	1,3
Power Supply Group "VD5" input and I/O pins at VDD5=3.6 to 5.25V	V_{IH}	2.0		5.25	V	1,3

Note 1) Values are based on VSS(GND)=0V.
Note 2) Regulations for pins under "VD3" (Power Supply Group column in "Pin Table").
Note 3) Regulations for pins under "VD5" (Power Supply Group column in "Pin Table").

Items	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Low Level Output Voltage							
Power Supply Group "VD3" output and I/O pins (Except XOUT pin)	I_{OL}=100µA	V_{OL}	0		0.2	V	1, 2
	I_{OL}=2mA	V_{OL}	0		0.4	V	1, 2
Power Supply Group "VD5" output and I/O pins	I_{OL}=100µA	V_{OL}	0		0.2	V	1, 3
	I_{OL}=4mA	V_{OL}	0		0.4	V	1
High Level Output Voltage							
Power Supply Group "VD3" output and I/O pins (Except XOUT pin)	I_{OH}= -100µA	V_{OH}	V_{DD33}-0.2		V_{DD33}	V	1, 2
	I_{OH}= -2mA	V_{OH}	2.4		V_{DD33}	V	1, 2
Power Supply Group "VD5" output and I/O pins	I_{OH}= -100µA	V_{OH}	V_{DD5}-0.2		V_{DD5}	V	1, 3
	I_{OH}= -4mA	V_{OH}	V_{DD5}×0.8		V_{DD5}	V	1, 3

Note 1) Values based on VSS(GND)=0V.
Note 2) Regulations for pins under "VD3" (Power Supply Group column in "Pin Table").
Note 3) Regulations for pins under "VD5" (Power Supply Group column in "Pin Table").

Items	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Input leakage Current		I_{LI}	-10		+10	µA	
Output leakage Current		I_{LO}	-25		+25	µA	

Items	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_I			10	pF
Output Pin Capacitance	C_O			10	pF
Input-Output Pin Capacitance	C_{IO}			10	pF

Items	Symbol	Min.	Typ	Max.	Unit	Note
Analog video Input Voltage (VINP pin)	V_{VINP}		1.25	1.4	Vp-p	1

Note 1) The above maximum values are for the setting of "R#28: ADCGAIN=2'b00."

● AC Characteristics

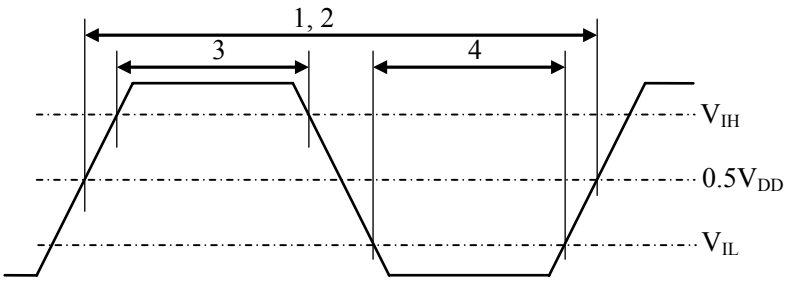
- Measurement Conditions

Input Voltage	0V / V_{DD33}
Input transition time	1ns (Transition time is specified between V_{DD33}×0.2 and V_{DD33}×0.8.)
Measurement reference voltage:	Input V_{IL}/V_{IH}
	Output V_{DD33}/2V
Output load capacitance	20pF

Clock Input

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	XIN Clock Frequency	f_{XIN}	6		40	MHz	
	XIN Clock Cycle Time	t_{XIN}	25		166	ns	
2	DTCKIN Clock Frequency	f_{DTCKIN}			40	MHz	
	DTCKIN Clock Cycle Time	t_{DTCKIN}	25			ns	
3	XIN, DTCKIN Clock High Level Pulse Width	t_{whCLK}	7.5			ns	
4	XIN, DTCKIN Clock Low Level Pulse Width	t_{wlCLK}	7.5			ns	
5	SYCLK Clock Frequency	f_{SYCLK}			83.16	MHz	1
	SYCLK Clock Cycle Time	t_{SYCLK}	12.03			ns	1
6	PLL Out Clock Frequency	f_{PLLO}	252		332.64	MHz	1
	PLL Out Clock Cycle Time	t_{PLLO}	3.01		3.96	ns	1
7	DCLK Clock Frequency	f_{DCLK}			40	MHz	2
	DCLK Clock Cycle Time	t_{DCLK}	25			ns	2

Note 1) SYCLK is a 1/4 frequency divided internal clock of PLL OUT.
Note 2) DCLK is a dot clock that is used internally.



Power Supply and Reset Input

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	RESET_N pin Input Time	t_{wRES}	10			µs	1
2	CPU Access Stand-by Time after RESET_N Negation	t_{wAW}	10 to 67			ms	
3	RESET_N Setup Time	t_{sRES}	0			ns	2
4	Power-on Time Difference (VDD33, VDDIN, AVDD)	t_{VSKWR}			1	s	3
5	Power-off Time Difference (VDD33, VDDIN, AVDD)	t_{VSKWF}			1	s	4
6	Power Rise Time	t_{VRISE}			200	ms	
7	VDD5Power-on/off Time Difference	t_{VSKWC}	-1			s	5
8	Core Power VOUT18 Rise Time	t_{vCORE}			300	µs	6
9	OCPEN pin Input Time (Initialization)	t_{wOCPE}	10			µs	
10	OCPEN pin Low Input Time (Abnormal)	t_{wOCPR}	0.4		10	ms	

Note 1) This is the time from when the following three conditions are met to the time when RESET_N rises: The voltage of the last power supply that was powered on reached at 3.0V, VOUT18 reached at 1.7V, and an input clock to XIN pin becomes stable.

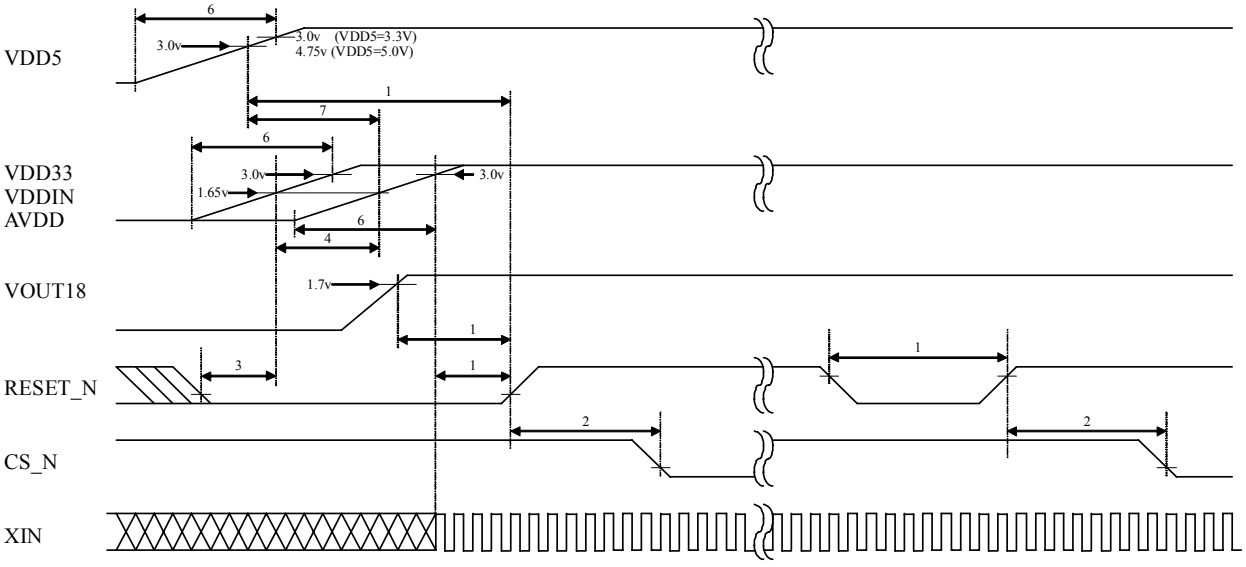
Note 2) This is the specification of the first power supply that was powered up, out of VDD33, VDDIN, and AVDD.

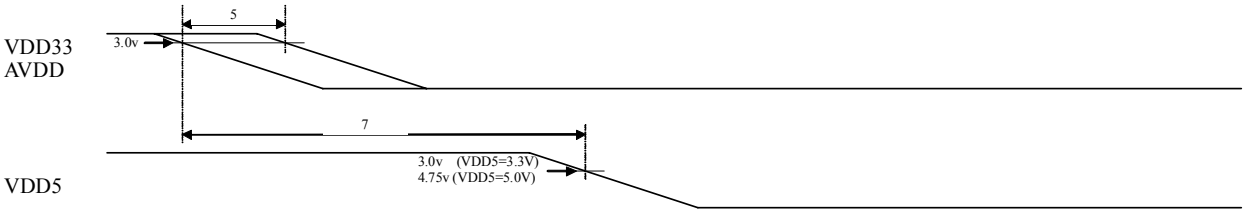
Note 3) It is recommended VDD33, VDDIN, and AVDD be turned on simultaneously. If one second or more time-difference occurs it may have an adverse effect on LSI's reliability.

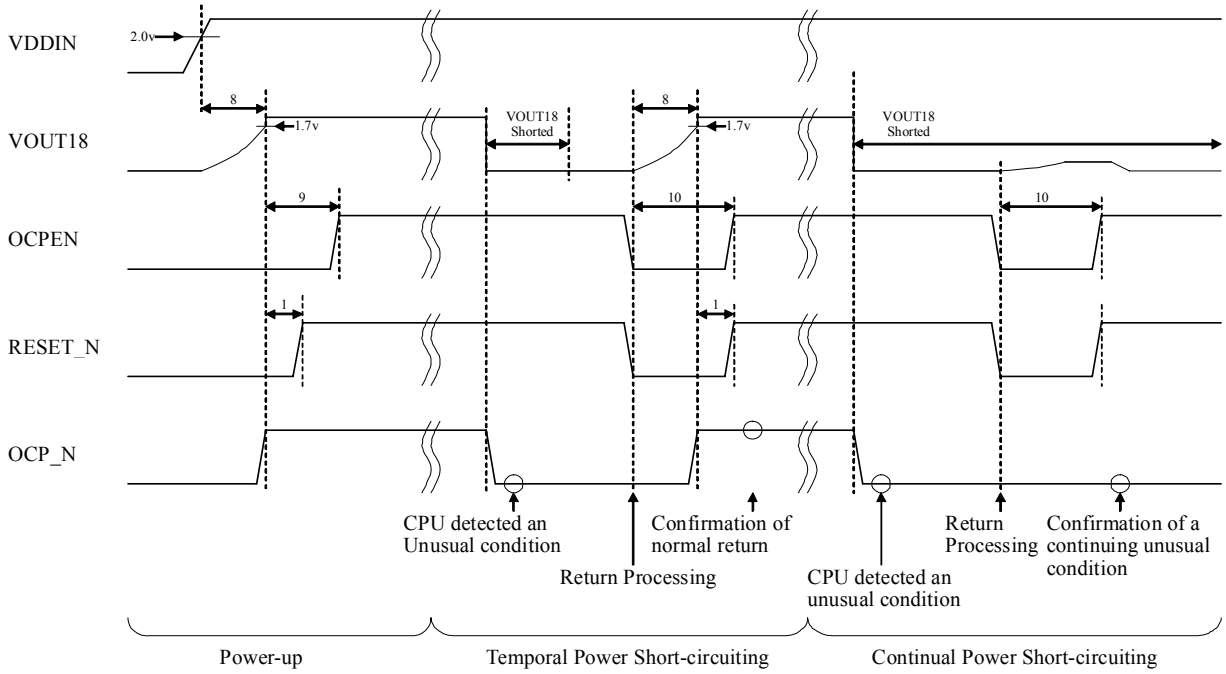
Note 4) It is recommended VDD33, VDDIN, and AVDD be turned off simultaneously. If it takes more than one second, it may have an adverse effect on LSI's reliability.

Note 5) It is possible to shutdown 3V power supply (VDD33, VDDIN, and AVDD) with 5V power (VDD5) applied.

Note 6) This is the value with four capacitors of 4.7µF connected to VOUT18 and VDDCORE pins.






VDDIN
VOUT18
OCPEN
RESET_N
OCP_N
2.0v
8
1.7v
VOUT18
Shorted
9
10
1
CPU detected an
Unusual condition
Confirmation of
normal return
Return Processing
CPU detected an
unusual condition
Return
Processing
Confirmation of a
continuing unusual
condition
Power-up
Temporal Power Short-circuiting
Continual Power Short-circuiting

CPU Interface

Parallel Interface

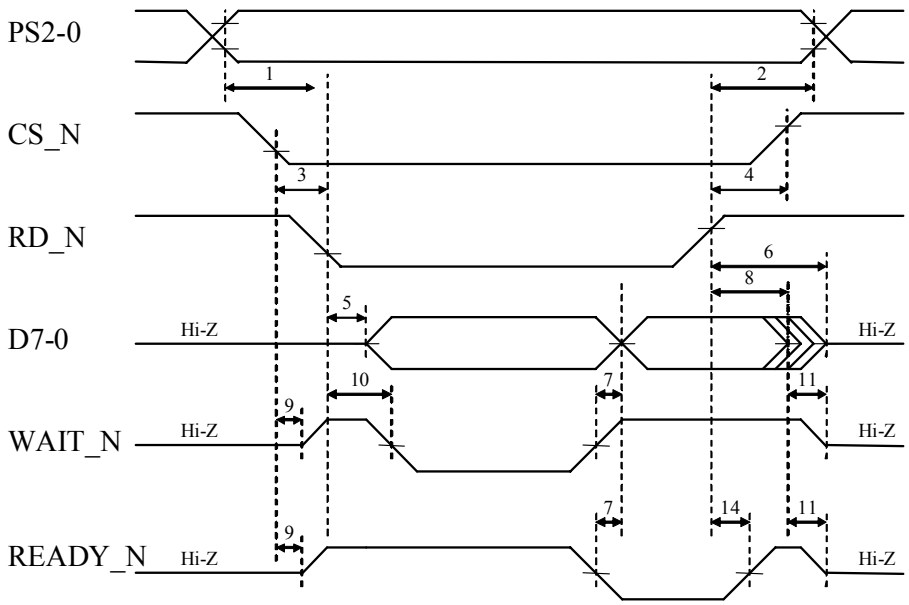
No.	Item	Code	Min.	Typ.	Max.	Unit	Note
1	PS2-0: setup time	t_{sA}	4			ns	1
2	PS2-0: hold time	t_{hA}	0				1
3	CS_N: setup time	t_{sCS}	0				2
4	CS_N: hold time	t_{hCS}	0				2
5	D7-0: output data turn on time	t_{onD}	0				
6	D7-0: output data turn off time	t_{offD}			30		
7	D7-0: output data valid delay time	t_{dD}			0		
8	D7-0: output data hold time	t_{hD}	0				
9	WAIT_N, READY_N: turn on time	t_{onWAIT}	0				
10	WAIT_N, READY_N: valid delay time	t_{dWAIT}			25		
11	WAIT_N, READY_N: turn off time	$t_{offWAIT}$			30		
12	D7-0: input data setup time	t_{sD}	t_{SYCLK}+15				
13	D7-0: input data hold time	t_{hD}	2				
14	READY_N: hold time	t_{hREADY}	0		30		
15	command pulse active time	t_{aCMD}	$2\times t_{SYCLK}$				3
16	command pulse inhibit time	t_{iCMD}	$4\times t_{SYCLK}$				3
17	command cycle time	t_{cCMD}	$6\times t_{SYCLK}$				3

Note 1) Regulations for WR_N and RD_N signals; however, in CS_N control, there are regulations for CS_N.

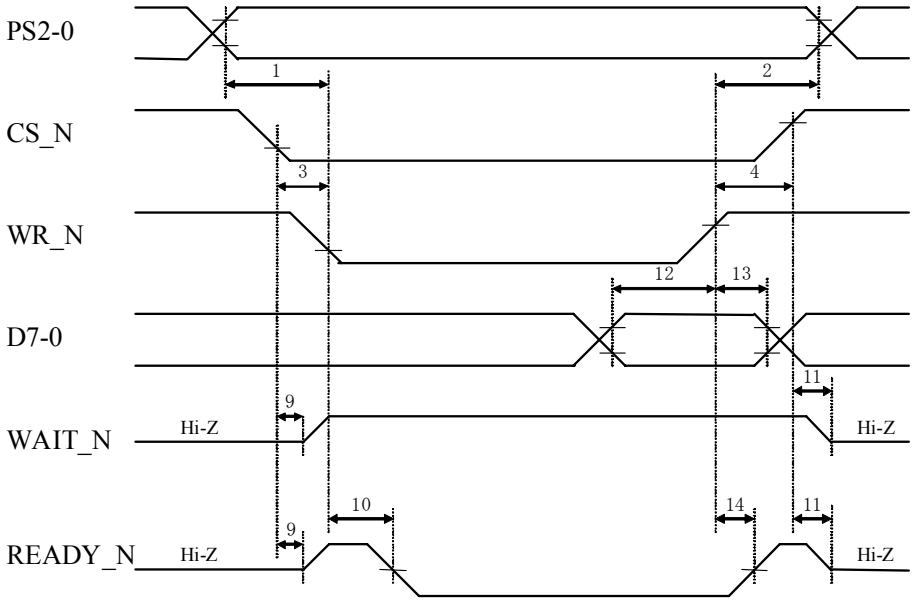
Note 2) Conditions that prove to be WR_N and RD_N controls. If these conditions are not met, these are for CS_N control.

Note 3) “command pulse” means a low active pulse obtained by performing OR operation between CS_N signal and each of WR_N and RD_N signals.

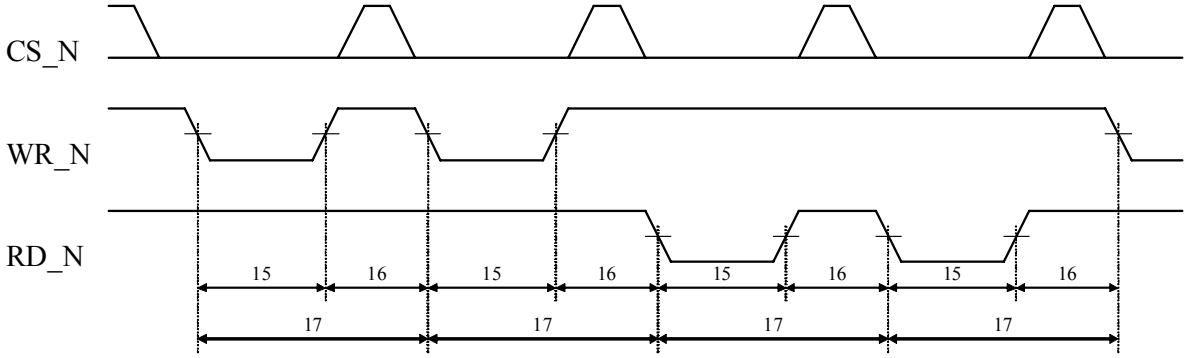
i) CPU Read Cycle



ii) CPU Write Cycle



iii) Access Cycle

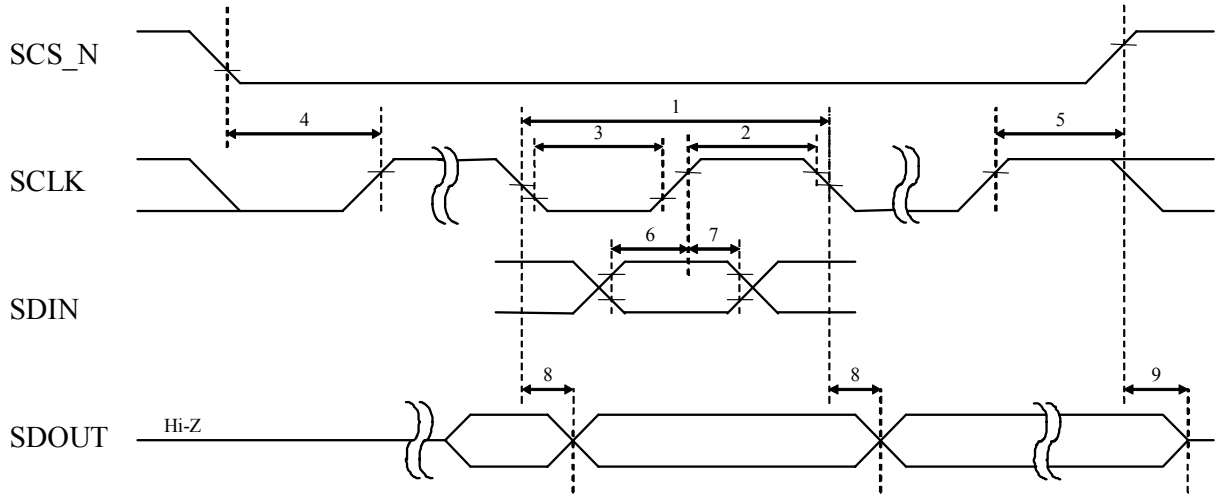


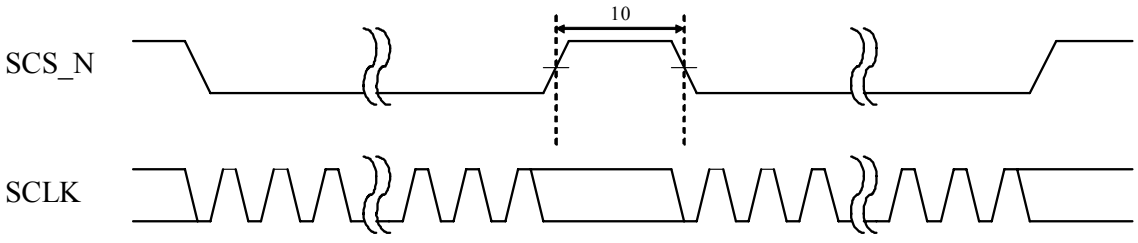
Serial interface chip select

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	SCLK Clock Cycle Time	t_{wSCLK}	200			ns	1
2	SCLK Clock High Level Pulse Width	t_{whSCLK}	100				1
3	SCLK Clock Low Level Pulse Width	t_{wlSCLK}	100				1
4	SCS_N: setup time	t_{sSCS}	25				
5	SCS_N: hold time	t_{hSCS}	25				
6	SDIN: setup time	t_{sSDI}	25				
7	SDIN: hold time	t_{hSDI}	25				
8	SDOUT: output data delay time	t_{dSDO}			100		2
9	SDOUT: turn off time	t_{offSDO}			20		
10	SCS_N: pulse inhibit time	t_{iSCS}			400		

Note 1) In the initialization, the 2-divided clock of XIN is used for the system clock. And, SCLK is sampled twice by the system clock. Therefore, the minimum value of t_{wSCLK} becomes XIN cycle×8 ($t_{XIN} \times 8$), and minimum values of t_{whSCLK} and t_{wlSCLK} become XIN cycle × 4 ($t_{XIN} \times 4$). Compare it with the value defined in the above table and use the larger value.

Note 2) In the initialization, the maximum value of t_{dSDO} becomes XIN cycle × 6+100ns ($t_{XIN} \times 6 + 100ns$).





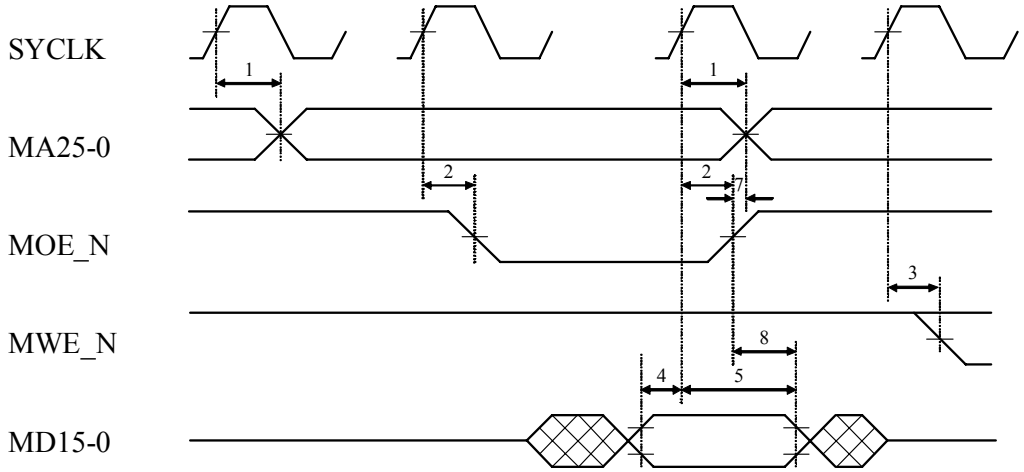
Pattern Memory Interface

No.	Items	Symbol	Min	Typ.	Max	Unit	Note
1	MA25-0: output delay time from SYCLK	t_{dMA}			14	ns	1
2	MOE_N: output delay time from SYCLK	t_{dOE}	2		14		1
3	MWE_N: output delay time from SYCLK	t_{dWE}	2		14		1
4	MD15-0 : input setup time to SYCLK	t_{sMD}	4				1
5	MD15-0 : input hold time from SYCLK	t_{hMD}	0				1
6	MD15-0 : output delay time from SYCLK	t_{dMD}			24		1
7	MA25-0: hold time from MOE_N	t_{hMAR}	0				
8	MD15-0 : input hold time from MOE_N, MA25-0	t_{hMDI}	0				
9	MA25-0: hold time from MWE_N	t_{hMAW}	0				
10	MD15-0 : hold time from MWE_N	t_{hMDO}	1				
11	MD15-0 : turn off time from MWE_N	t_{offMDO}	1		10		
12	Output turn off/on time from RAHZ_N	$t_{on/offRA}$			25		

Note 1) SYCLK is an internal clock.

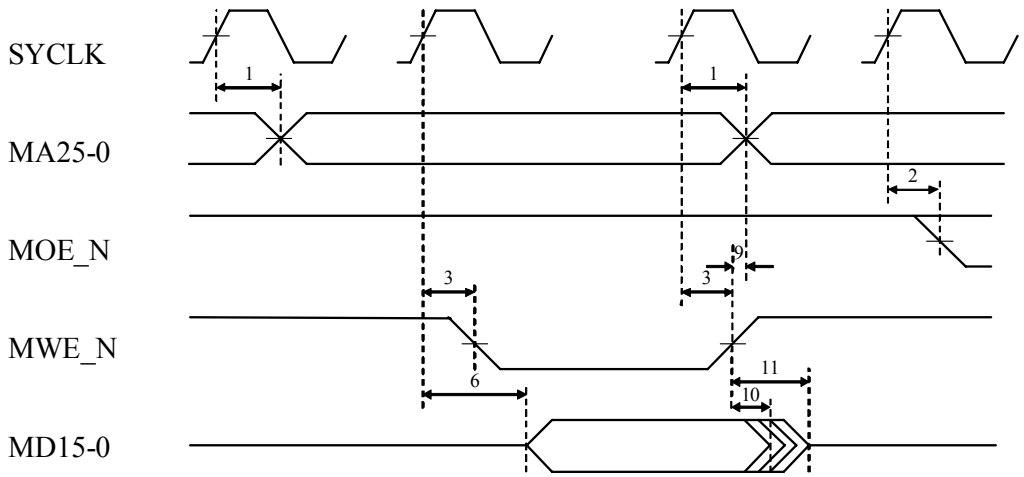
Memory access cycle

i) Random read cycle



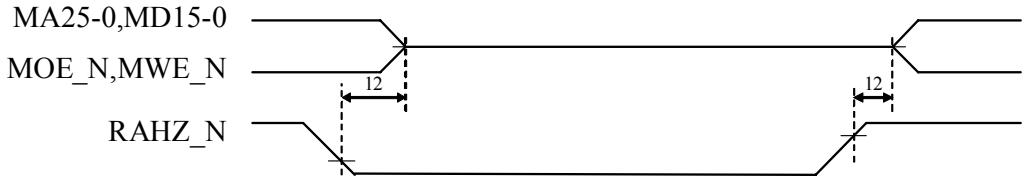
Note: After a read access, values of MA25-0, MOE_N are held until the pattern memory is accessed again.

ii) Write Cycle



Note: After a write access, the value of MA25-0 is held until the pattern memory is accessed again.

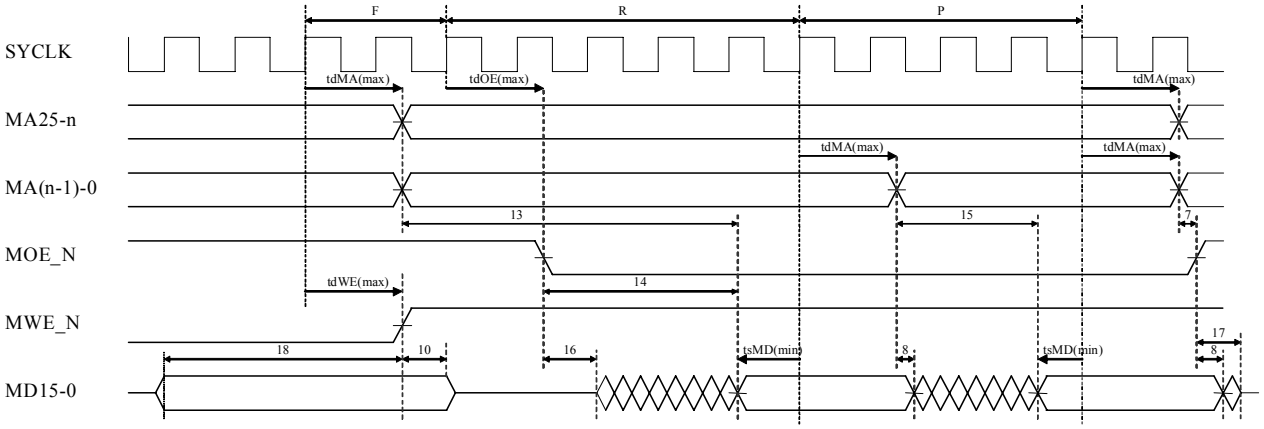
iii) RAHZ_N

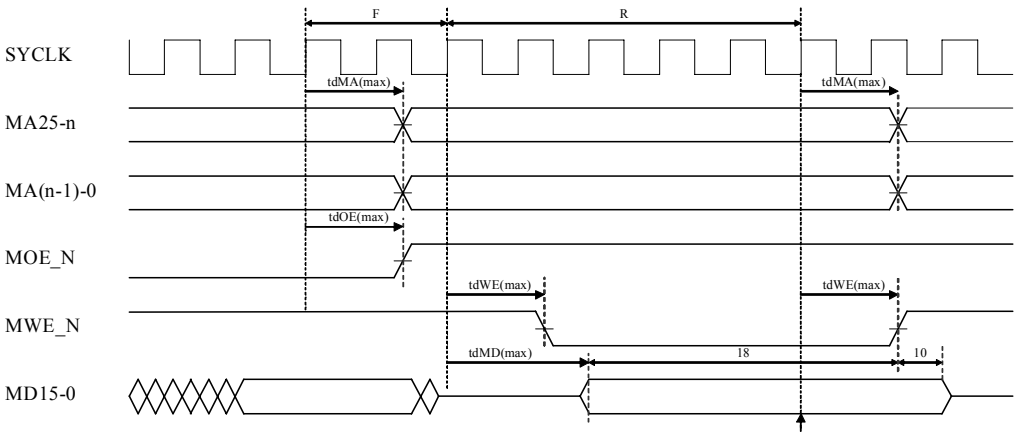


Note: The AC characteristics of an external memory connecting to VC1E must meet the following conditions.
(The following conditions are the values converted from the AC characteristics of the VC1E pattern memory; they do not guarantee the following specifications directly. In addition, the item names below are those mainly for an externally-connected memory.)
"F", "R", and "P" in the below are as follows.

- F =(R#2:FLTIM[1:0]+1) Number of Floating Clocks
- R =(R#3:RDM[3:0]+1) Number of Random Access Clocks,
- P =(R#3:PAG[2:0]+1) Number of Page Mode Access Clocks

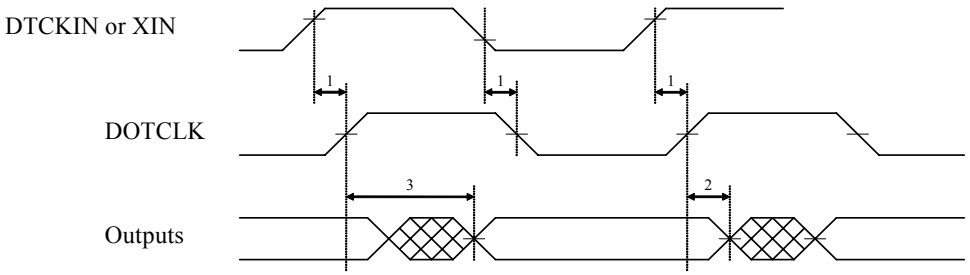
No.	Items	Conditions
13	Address, Access Time	It should be (F + R) * t_{SYCLK} – t_{dMA}(max) – t_{sMD}(min) or lower
14	Output Enable Time	It should be R * t_{SYCLK} – t_{dOE}(max) – t_{sMD}(min) or lower
15	Page Mode Access Time	It should be P * t_{SYCLK} – t_{dMA}(max) – t_{sMD}(min) or lower
16	Data Turn On Time	It should be 0[ns] or over
17	Data Turn Off Time	It should be F * t_{SYCLK} - t_{dOE}(max) + t_{dWE}(min) or lower
18	Data Setup Time	It should be R * t_{SYCLK} - t_{dMD}(max) + t_{dWE}(min) or lower





Display Timing Signals

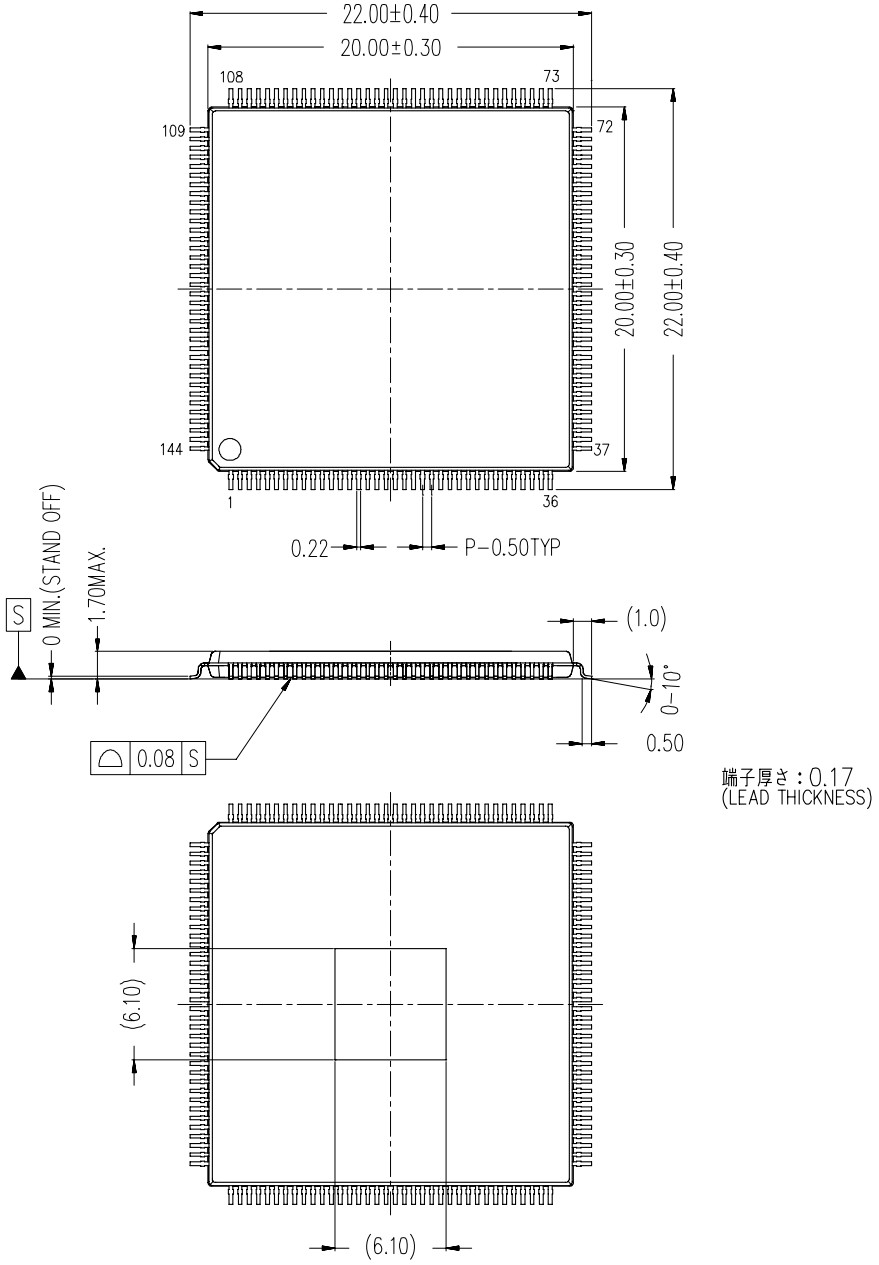
No.	Items	Symbol	Min	Typ	Max	Unit	Note
1	DOTCLK: delay time	t_{dDOTC}			26	ns	
2	VSYNC_N, HCSYNC_N, BLANK_N, DR5-0, DG5-0, DB5-0, CLKV, STARTH, STARTV, LOADH, POL, OUTENV: output hold time	t_{hDISP}	-4			ns	
3	VSYNC_N, HCSYNC_N, BLANK_N, DR5-0, DG5-0, DB5-0, CLKV, STARTH, STARTV, LOADH, POL, OUTENV: output delay time	t_{dDISP}			4	ns	



Note: the above figure shows a state in which DOTCLK is not inverted.

■ Package Outlines

C-PK144VP3-4



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

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PRECAUTIONS AND INSTRUCTIONS FOR SAFETY

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Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings (current, voltages, safety operation ranges, temperature, etc.). Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causes of breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins. In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, in case of the occurrence of unusual speaker output due to a malfunction or failure. A speaker radiates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat radiation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoke, or ignition of a speaker even if it is used within the rated input value.

⚠ CAUTION

Prohibited	Do not use Yamaha products in a position close to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of user to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as overcurrent protection circuit etc. so that it does not keep on flowing during operation or failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the start of the protection circuit.
Instructions	Use a stable power supply. The use of unstable power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the possibility of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation. Therefore, please take care not to touch an operating device directly.

Notice The specifications of this product are subject to improvement changes without prior notice.

AGENT

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